AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings of claims in the application.

LISTING OF THE CLAIMS:

1. (Original) A terminal apparatus comprising a microprocessor having a DSP function (600) and a CPU function integrated with each other as a single bus master, and an internal memory space and an external memory space integrated as a single memory space, wherein

the DSP function includes a plurality of internal memories (602, 603) and a plurality of buses (604, 605) for connecting said internal memories for executing the non-recursive filter operation constituting a basic operation of the digital signal processing at the rate of one cycle per tap,

and said CPU function (600) is capable of executing a basic instruction for any of such operations as calculation, internal memory access and data transfer at the rate of an instruction per cycle, and thereby capable of compiling a program written in a high-level language into said basic instruction and executing said basic instruction efficiently.

2. (Original) A terminal apparatus according to Claim 1, further comprising an integrated peripheral circuit (503) accessible from both the DSP function (600) and the CPU function (600).

3. (Original) A terminal apparatus according to Claim 1,

wherein said microprocessor comprises a directly-coupled interface (1006) for an external memory having high-speed access mode.

4. (Original) A terminal apparatus according to Claim 1,

wherein said internal memory has built therein an audio coding/decoding program and a communication path coding/decoding program (801), and said external memory has stored therein a communication protocol program and a user interface program (803).

5. (Original) A terminal apparatus according to Claim 1,

wherein said microprocessor comprises a cache memory (704) and means for controlling the cache memory.

6. (Original) A terminal apparatus according to Claim 2,

wherein said microprocessor (1300) is capable of transferring a plurality of input-output samples collectively from a serial input-output circuit to the internal memory and the external memory.

7. (Original) A terminal apparatus according to Claim 1,

wherein said microprocessor comprises an interface (1206) directly connected to an external DRAM, said interface being directly accessible by the function capable of executing the non-recursive filter calculation providing the basic operation of digital signal processing at the rate of one cycle per tap.

8. (Original) A method of configuring a high-level language compiler for generating a microprocessor program used for the terminal apparatus according to Claim 1, wherein at least an address register for a digital signal processor realizing the DSP function is mapped to a subset of registers for a central processing unit realizing the CPU function thereby to deliver at least an argument to said subset of the registers of said central processing unit.

9. (Original) A terminal apparatus for effecting radio communication by exchanging data with a base station, comprising:

a data processing unit (500) for executing a program stored in memory; and

a memory including an area (801) storing a program for performing the audio coding/encoding process, an area storing a program for performing the speech decoding process, an area storing a program for performing the channel decoding process, an area (803) storing a program for controlling the communication protocol with the base station, and an area storing a program for controlling the interface with the user;

wherein each of said areas of said memory is arranged in an address space of said data processing unit.

10. (Original) A terminal apparatus according to Claim 9, wherein said data processing unit includes a digital signal processor for executing the audio coding process, the speech decoding process, the communication path coding process and the communication path decoding, and a central processing unit for controlling the communication protocol with the base station and also controlling the interface with the user, wherein said digital signal processor and said central processing unit are formed on a single semiconductor substrate.

11. (Currently Amended) A terminal apparatus according to Claim 9 ~~or 10~~, wherein said memory built in said data processing unit has said area storing a program for executing the audio coding process, said area storing a program for executing the speech decoding process, said area storing a program for executing the communication path coding, and said area storing a program for executing the communication path decoding.

12. (Currently Amended) A terminal apparatus according to ~~any one of Claims 9 and 10~~ claim 9, wherein a memory external to said data processing unit has an area storing a program for controlling the communication protocol with the base station and an area storing a program for controlling the interface with the user.

13. (Currently Amended) A terminal apparatus according to Claim 9 ~~or 10~~, wherein said data processing unit includes, in the address space of said central processing unit, a serial input-output circuit for interfacing with an analog/ digital converter circuit and a digital/analog converter circuit.

Claim 14 (Cancelled)

15. (New) A terminal apparatus comprising:

a microprocessor having a DSP function and a CPU function,

wherein the DSP function and a CPU function are integrated with each other as a single bus master, and an internal memory space and an external memory space being integrated as single memory space,

wherein the DSP function is capable of executing a non-recursive filter operation constituting a basic operation of a digital signal processing at a rate of one cycle per tap,

wherein the CPU function is capable of executing a basic instruction for any of such operation as calculation, internal memory access and data transfer at the rate of one cycle per tap.